12-Channel Self Calibration Capacitive Touch Sensor

Specification V1

Preliminary

For details see TSM12 datasheet

1 Specification

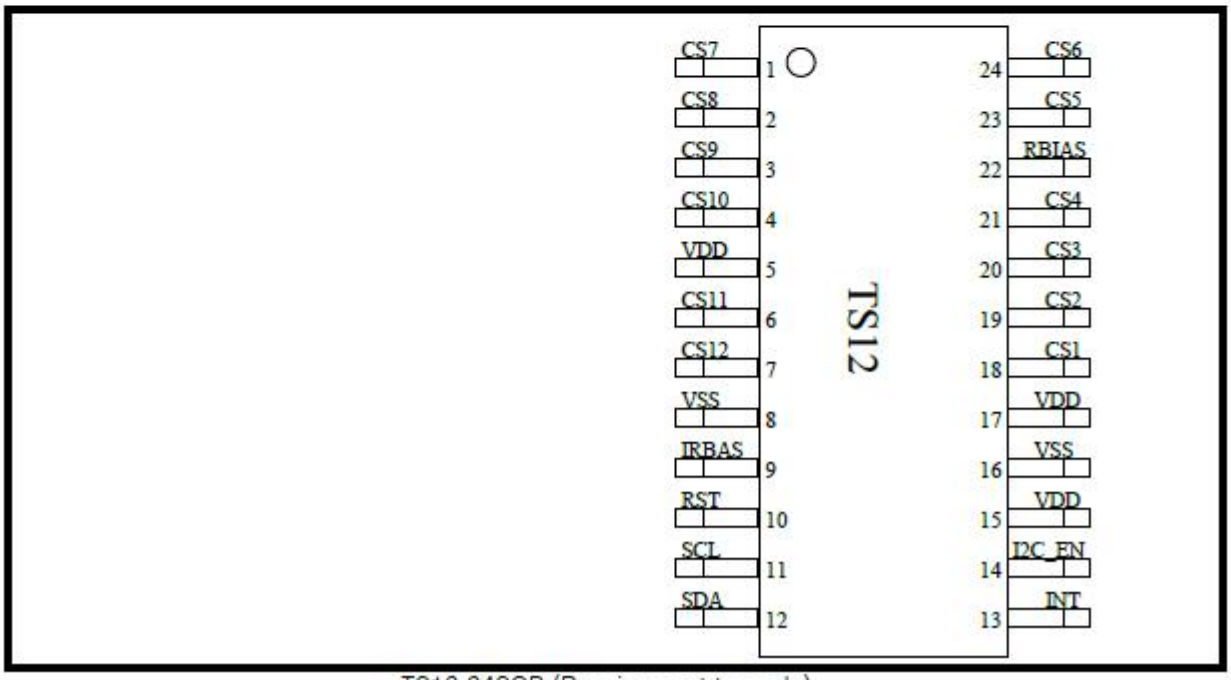
1.1 General Feature

- 12-Channel capacitive sensor with auto sensitivity calibration
- Selectable output operation (single mode / multi-mode)
- Independently adjustable in 8 step sensitivity
- Touch intensity can be detectable within 3 steps (Low, Middle and High)
- Adjustable internal frequency with external resister
- Adjustable response time and interrupt level by the control registers
- I2C serial interface
- Embedded high frequency noise elimination circuit
- Embedded power key function on channel 1 for mobile phone application
- RoHS compliant 24SOP package

1.2 Application

- Mobile application (mobile phone / PDA / PMP etc)
- Membrane switch replacement
- Sealed control panels, keypads
- Door key-lock matrix application
- Touch screen replacement application

1.3 Package (24SOP)



TS12 24SOP (Drawings not to scale)

2 Pin Description (24SOP)

PIN No.	Name	I/O	Description	Protection
1	CS7	Analog Input	CH7 capacitive sensor input	VDD/GND
2	CS8	Analog Input	CH8 capacitive sensor input	VDD/GND
3	CS9	Analog Input	CH9 capacitive sensor input	VDD/GND
4	CS10	Analog Input	CH10 capacitive sensor input	VDD/GND
5	VDD	Digital Input	–	VDD/GND
6	CS11	Analog Input	CH11 capacitive sensor input	VDD/GND
7	CS12	Analog Input	CH12 capacitive sensor input	VDD/GND
8	VSS	Ground	Supply ground	VDD
9	IRBIAS	Analog Input	Internal I2C clk frequency adjust input	VDD/GND
10	RST	Digital Input	System reset (High reset)	VDD/GND
11	SCL	Digital Input	I2C clock input	VDD/GND
12	SDA	Digital Input/Output	I2C data (Open drain)	VDD/GND
13	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
14	I2C_EN	Digital Input	I2C enable(Low enable)	VDD/GND
15	VDD	Digital Input	–	VDD/GND
16	VSS	Ground	Supply ground	VDD
17	VDD	Digital Input	–	VDD/GND
18	CS1	Analog Input	CH1 capacitive sensor input	VDD/GND
19	CS2	Analog Input	CH2 capacitive sensor input	VDD/GND
20	CS3	Analog Input	CH3 capacitive sensor input	VDD/GND
21	CS4	Analog Input	CH4 capacitive sensor input	VDD/GND
22	RBIAS	Analog Input	Internal bias adjust input	VDD/GND
23	CS5	Analog Input	CH5 capacitive sensor input	VDD/GND
24	CS6	Analog Input	CH6 capacitive sensor input	VDD/GND

3 Absolute Maximum Rating

Battery supply voltage	5.0V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	2000V	VDD
		2000V	VSS
		2000V	P to P
M.M	Pos / Neg	200V	VDD
		200V	VSS
		200V	P to P
C.D.M	Pos / Neg	500V	DIRECT
		800V	

4.2 Latch-up Characteristics

Mode	Polarity	Max	Test Step
I Test	Positive	200mA	25mA
	Negative	−200mA	
V supply over 5.0V	Positive	8.0V	1.0V

5 Electrical Characteristics

▪ V_{DD}=3.3V, Rb=510k, (Unless otherwise noted), T_A = 25℃

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Operating supply voltage	V_{DD}		2.5	3.3	5.0	V
Current consumption Note1	I_{DD}	V_{DD}= 3.3V R_B=510k	–	80	130	μA
		V_{DD}= 5.0V R_B=510k	–	200	315	
	I_{DD_I2C}	V_{DD}= 3.3V R_B=510k R_{I2C} =20k	–	1.5	–	mA
		V_{DD}= 5.0V R_B=510k R_{I2C} =30k	–	2.3	–	
		IDD_I2C Disable	–	–	1	μA
Output maximum sink current	I_{OUT}	T_A = 25℃	–	–	4.0	mA
Sense input capacitance range Note2	C_S		–	10	100	pF
Sense input resistance range	R_S		–	200	1000	Ω
Minimum detective capacitance difference	ΔC	Cs = 10pF, C_{DEG} = 200pF (I2C default sensitivity select)	0.2	–	–	pF
Output impedance (open drain)	Zo	ΔC > 0.2pF, Cs = 10pF, (I2C default sensitivity select)	–	12	–	Ω
		ΔC < 0.2pF, Cs = 10pF, (I2C default sensitivity select)	–	30M	–	
Self calibration time after system reset	T_{CAL}	V_{DD} = 3.3V R_B = 510k	–	100	–	ms
		V_{DD} = 5.0V R_B = 510k	–	80	–	
Recommended bias resistance range Note3	R_B	V_{DD} = 3.3V	200	510	820	kΩ
		V_{DD} = 5.0V	330	620	1200	
Maximum bias capacitance	C_{B_MAX}		–	820	1000	pF

Note 1 : In case of SCL frequency is 500kHz.

Note 2 : The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern.

Note 3 : The lower R_B is recommended in noisy condition.

7.6 First Byte

7.6.1 Slave Address

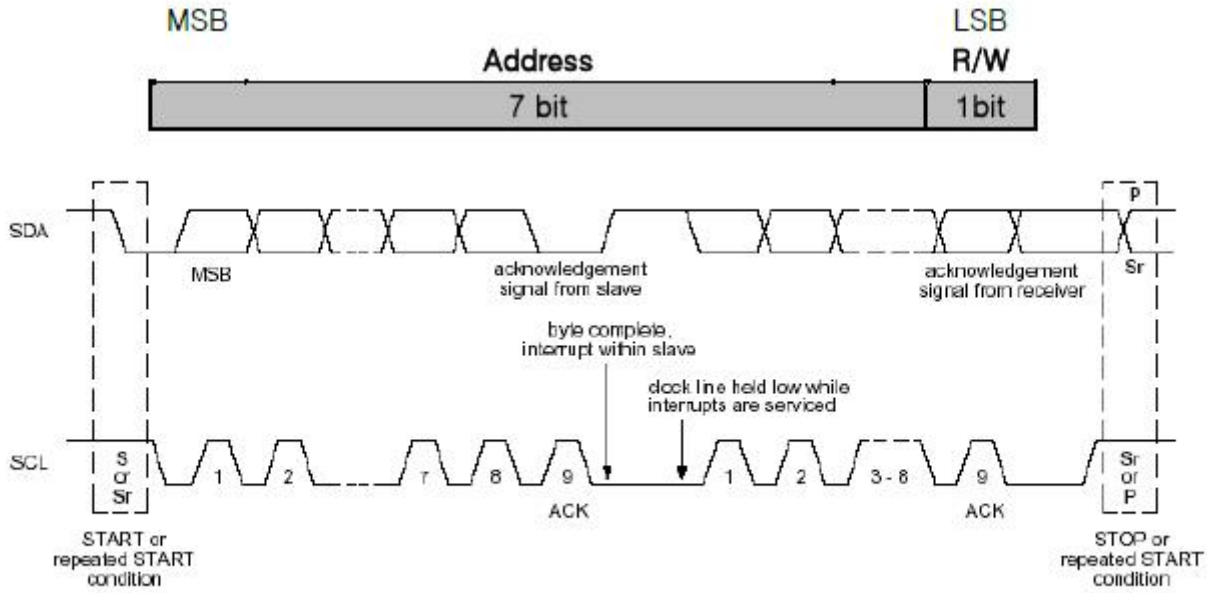
It is the first byte from the start condition. It is used to access the slave device.

TS12 Chip Address : 7bit

Address
0xF0

7.6.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.

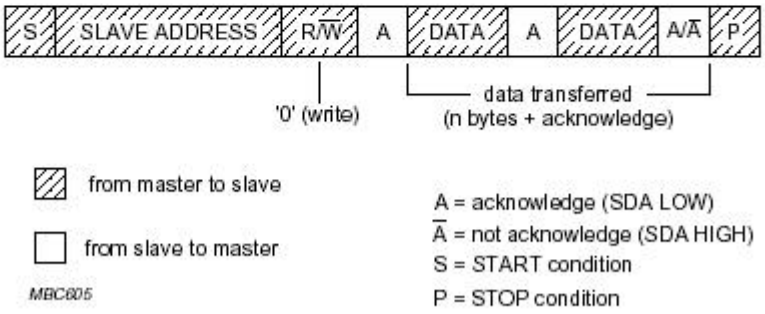


7.7 Transferring Data

7.7.1 Write Operation

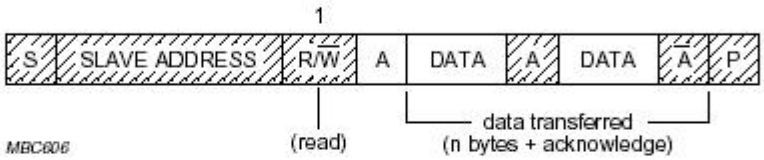
The byte sequence is as follows:

- the first byte gives the device address plus the direction bit (R/W = 0).
- the second byte contains the internal address of the first register to be accessed.
- the next byte is written in the internal register. Following bytes are written in successive internal registers.
- the transfer lasts until stop conditions are encountered.
- the TS12 acknowledges every byte transfer.

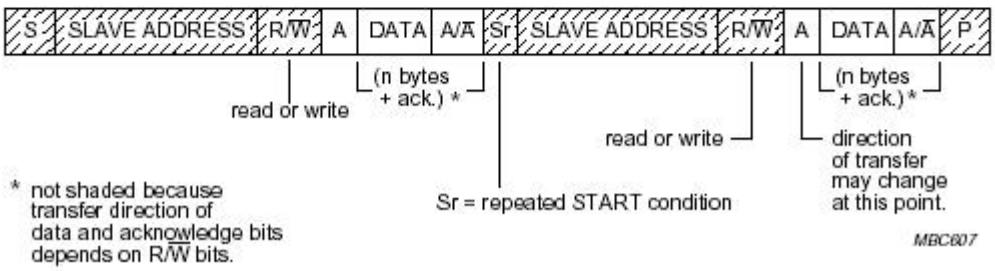


7.7.2 Read Operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



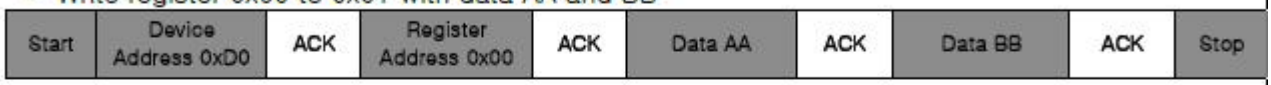
7.7.3 Read/Write Operation



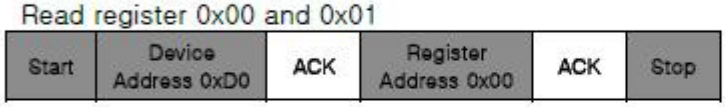
7.8 I²C write and read operations in normal mode

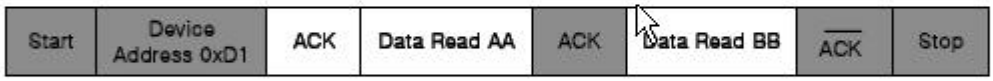
The following figure represents the I²C normal mode write and read registers.

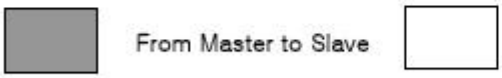
☞ Write register 0x00 to 0x01 with data AA and BB



Read register 0x00 and 0x01







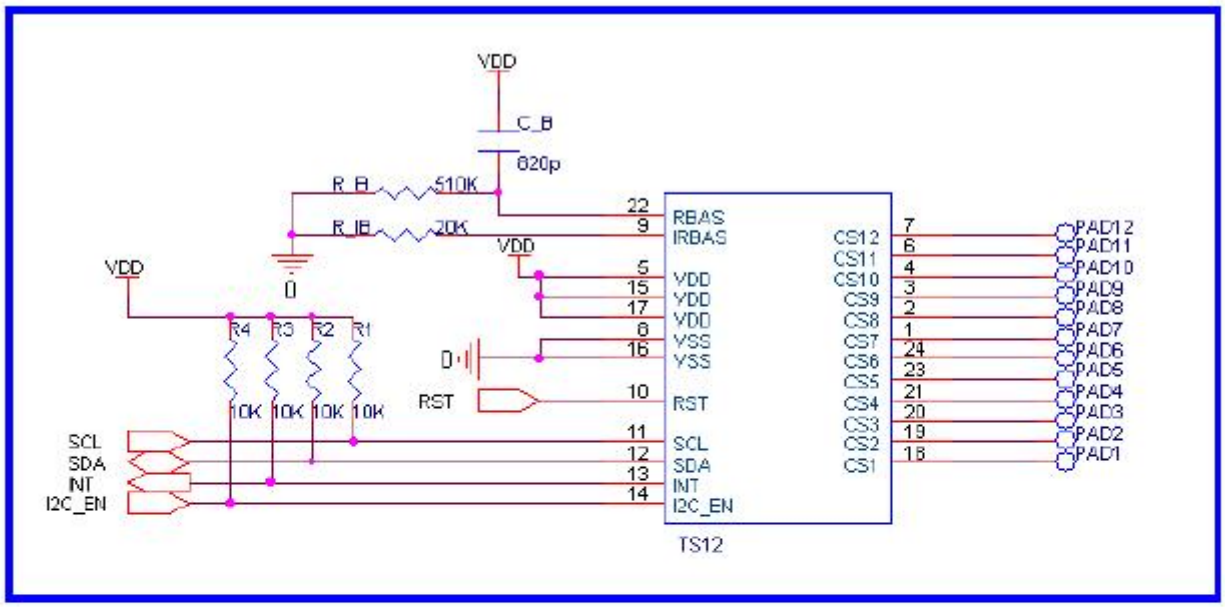
8 TS12 Register List

- Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.
- Note: The bit0 and bit1 of CTRL2 register must be written by 0b11 after power on during an initialize phase. (Refer to the chapter 9. initialize flow)
- Note: HS (High Sensitivity) / MS (Middle Sensitivity) / LS (Low Sensitivity)
- Note: Low Output (light touch) / Middle Output (middle touch) / High Output (hard touch)

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sensitivity1	02h	1011 1011	Ch2HL	Ch2M			Ch1HL	Ch1M		
Sensitivity2	03h	1011 1011	Ch4HL	Ch4M			Ch3HL	Ch3M		
Sensitivity3	04h	1011 1011	Ch6HL	Ch6M			Ch5HL	Ch5M		
Sensitivity4	05h	1011 1011	Ch8HL	Ch8M			Ch7HL	Ch7M		
Sensitivity5	06h	1011 1011	Ch10HL	Ch10M			Ch9HL	Ch9M		
Sensitivity6	07h	1011 1011	Ch12HL	Ch12M			Ch11HL	Ch11M		
CTRL1	08h	0010 0010	MS	FTC		ILC		RTC		
CTRL2	09h	0000 01XX	0	0	0	0	SRST	IDLE	1	1
Ref_rst1	0Ah	1111 1110	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Ref_rst2	0Bh	0000 1111	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Ch_hold1	0Ch	1111 1110	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Ch_hold2	0Dh	0000 1111	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Cal_hold1	0Eh	0000 0000	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Cal_hold2	0Fh	0000 0000	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Output1	10h	0000 0000	OUT4		OUT3		OUT2		OUT1	
Output2	11h	0000 0000	OUT8		OUT 7		OUT6		OUT5	
Output3	12h	0000 0000	OUT12		OUT11		OUT10		OUT9	

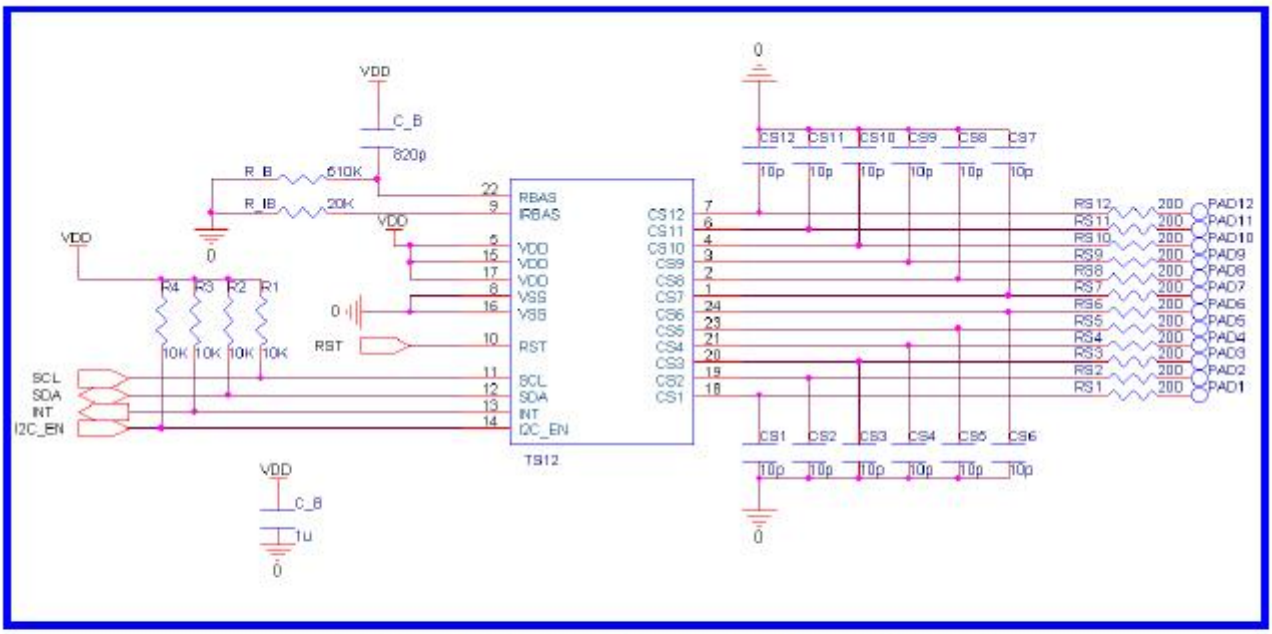
10.1 Application Example in clean power environment



TS12 Application Example Circuit (Clean power environment)

- In PCB layout, R_B should not be placed on touch pattern. If not, C_B has to be connected. The R_B pattern should be routed as short as possible.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS12.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The TS12 is reset if RST Pin is high. (See 6.3 Reset implementation chapter)

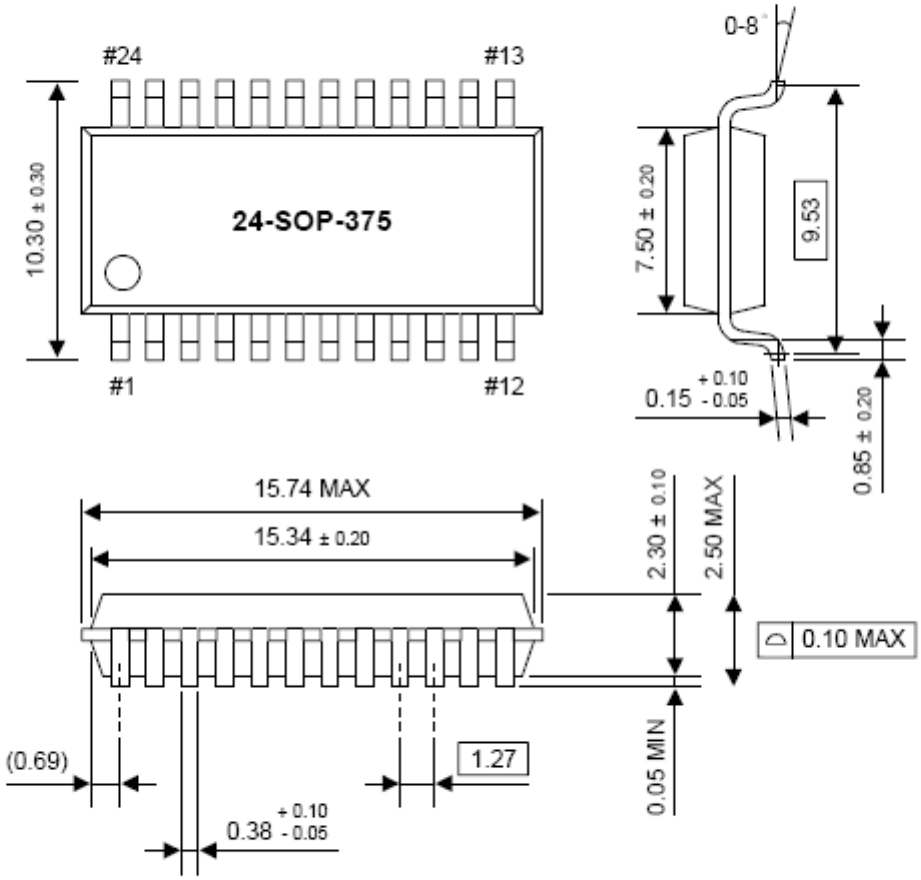
10.2 Application Example in noisy environment



TS12 Application Example Circuit (Noisy environment)

- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The smaller R_B is recommended in noisy environments.

11 MECHANICAL DRAWING



NOTE: Dimensions are in millimeters.

LIFE SUPPORT POLICY

touchSEMI PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES NOR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF THE EPSILLON COMPANY.
touchSEMI IS MEMBER OF EPSILLON COMPANY.

touchSEMI Sales Office

touchSEMI

www.touchsemi.com

Tel.: (+420) 212247491
Fax: (+420) 212247466

Na mokrině 45, 130 00 Prague 3
Czech Republic, EU