TS06

6-Channel Self Calibration Capacitive Touch Sensor

SPECIFICATION V1.0

1 Specification

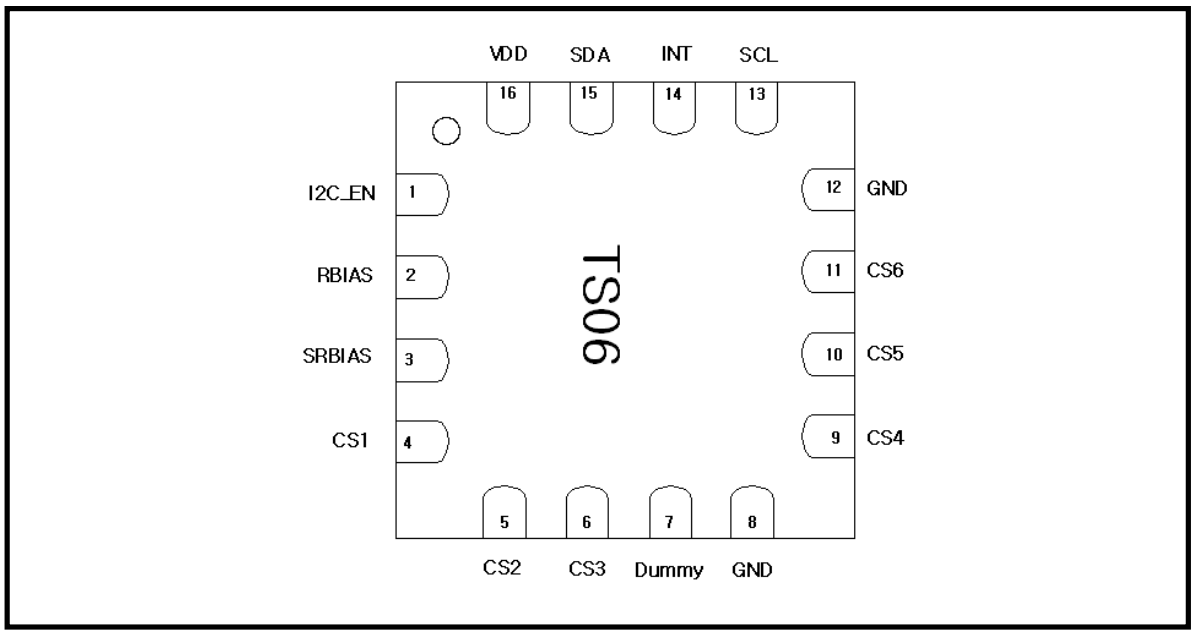
1.1 General Feature

- 6-Channel capacitive sensor with auto sensitivity calibration
- I^2C serial interface
- Selectable output operation (single mode / multi-mode)
- Independently adjustable in 16 step sensitivity
- Adjustable internal frequency with external resister
- Adjustable response time by the control registers
- Embedded high frequency noise elimination circuit
- Available LED drive up to 3 ports
- Controllable LED luminance
- Available tact switch input up to 5 channels
- IDLE mode to save the current consumption
- Programmable wake up sequence from IDLE mode
- RoHS compliant 16QFN package

1.2 Application

- Mobile application (mobile phone / PDA / PMP / MP3 etc)
- Membrane switch replacement
- Sealed control panels, keypads

1.3 Package (16 QFN)



TS06 16QFN (Drawings not to scale)

2 Pin Description (16QFN)

PIN No.	Name	I/O	Description	Protection
1	I2C_EN	Digital Input	I^2C enable(Low enable)	VDD/GND
2	RBIAS	Analog Input	Internal bias adjust input	VDD/GND
3	SRBIAS	Analog Input	IDLE Mode Internal bias adjust input	VDD/GND
4	CS1	Analog Input	CH1 capacitive sensor input I^2C slave ID selection input [Note 1]	VDD/GND
5	CS2	Analog Input	CH2 capacitive sensor input Tact switch input [Note 2]	VDD/GND
6	CS3	Analog Input	CH3 capacitive sensor input Tact switch input [Note 2]	VDD/GND
7	Dummy	Analog Input	Internal noise monitoring input Do not connect to anywhere	VDD/GND
8	GND	Ground	Supply ground	VDD
9	CS4	Analog Input /Digital Output	CH4 capacitive sensor input Tact switch input [Note 2] LED Drive output (Open drain) [Note 3]	VDD/GND
10	CS5	Analog Input /Digital Output	CH5 capacitive sensor input Tact switch input [Note 2] LED Drive output (Open drain) [Note 3]	VDD/GND
11	CS6	Analog Input /Digital Output	CH6 capacitive sensor input Tact switch input [Note 2] LED Drive output (Open drain) [Note 3]	VDD/GND
12	GND	Ground	Supply ground	VDD
13	SCL	Digital Input	I^2C clock input	VDD/GND
14	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
15	SDA	Digital Input/Output	I^2C data (Open drain)	VDD/GND
16	VDD	Power	Power (2.5V~5.0V)	GND

Note 1: Refer to chapter 7. I^2C Interface.
Note 2: Refer to chapter 6.3 CS implementation for tact switch input.
Note 3: Refer to chapter 6.4 CS implementation for LED drive output.

3 Absolute Maximum Rating

Maximum supply voltage	5.0V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Minimum Level	Reference
H.B.M	Pos / Neg	2000V	VDD
		2000V	GND
		2000V	P to P
M.M	Pos / Neg	200V	VDD
		200V	GND
		200V	P to P
C.D.M	Pos / Neg	500V	DIRECT
		800V	

4.2 Latch-up Characteristics

Mode	Polarity	Minimum Level	Test Step
I Test	Positive	200mA	25mA
	Negative	−200mA	
V supply over 5.0V	Positive	8.0V	1.0V

5 Electrical Characteristics

▪ V_{DD}=3.0V, Rb=510k (Unless otherwise noted), T_A = 25℃

Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Operating supply voltage	V_{DD}		2.5	3.0	5.0	V
Current consumption [Note4]	I_{DD}	V_{DD}= 3.0V R_B=510k R_{SB}=0	–	30	50	μA
		V_{DD}= 5.0V R_B=510k R_{SB} =0	–	80	130	
		V_{DD}= 3.0V R_B=510k R_{SB} =2M	–	8	–	
		V_{DD}= 5.0V R_B=510k R_{SB} =2M	–	28	–	
	I_{DD_I2C}	V_{DD}= 3.0V (1M Bps)	–	1.8	2.2	mA
		V_{DD}= 5.0V (1M Bps)	–	2.8	3.4	
Digital output maximum sink current	I_{OUT}	T_A = 25℃ (Normal I^2C Output)	–	–	4.0	mA
LED drive output sink current per 1channel	I_{LED_OUT}	T_A = 25℃ (LED Drive Output)	–	–	20.0	mA
LED drive output total sink current	I_{LED_TOT}	T_A = 25℃ (LED Drive Output)	–	–	30.0	mA
Tact switch interface input internal pull-up current	I_{TACT}	V_{DD}= 5.0V, T_A = 25℃	–	8	–	μA
Start supply voltage for internal reset	V_{DD_RST}	T_A = 25℃, R_B=510k	–	–	0.3·V_{DD}	V
Sense input capacitance range [Note5]	C_S		–	–	100	pF
Minimum detective capacitance difference	ΔC	Cs = 10pF (I^2C default sensitivity select)	0.2	–	–	pF
Output impedance (open drain)	Zo	ΔC > 0.2pF, Cs = 10pF, (I^2C default sensitivity select)	–	12	–	Ω
		ΔC < 0.2pF, Cs = 10pF, (I^2C default sensitivity select)	–	30M	–	
Self calibration time after system reset	T_{CAL}	V_{DD} = 3.0V R_B = 510k	–	100	–	ms
		V_{DD} = 5.0V R_B = 510k	–	80	–	
Sense input resistance range	R_S		–	200	1000	Ω
Recommended bias resistance range [Note6]	R_B	V_{DD} = 3.0V	200	510	820	kΩ
		V_{DD} = 5.0V	330	620	1200	
IDLE mode resistor range	R_{SB}		–	2	3	MΩ
Maximum bias capacitance	C_{B_MAX}		–	820	1000	pF

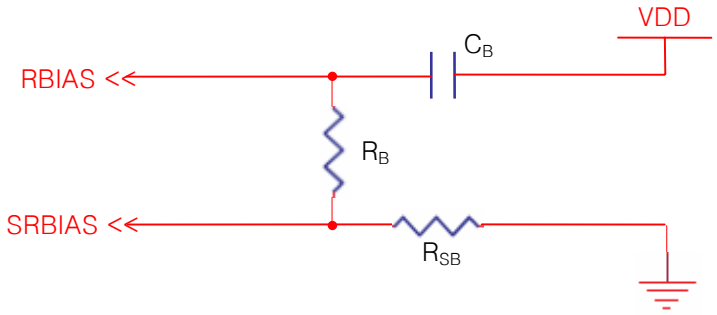
Note 4 : Maximum communication speed is 1Mbps.

Note 5 : The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern.

Note 6 : The lower R_B is recommended in noisy condition.

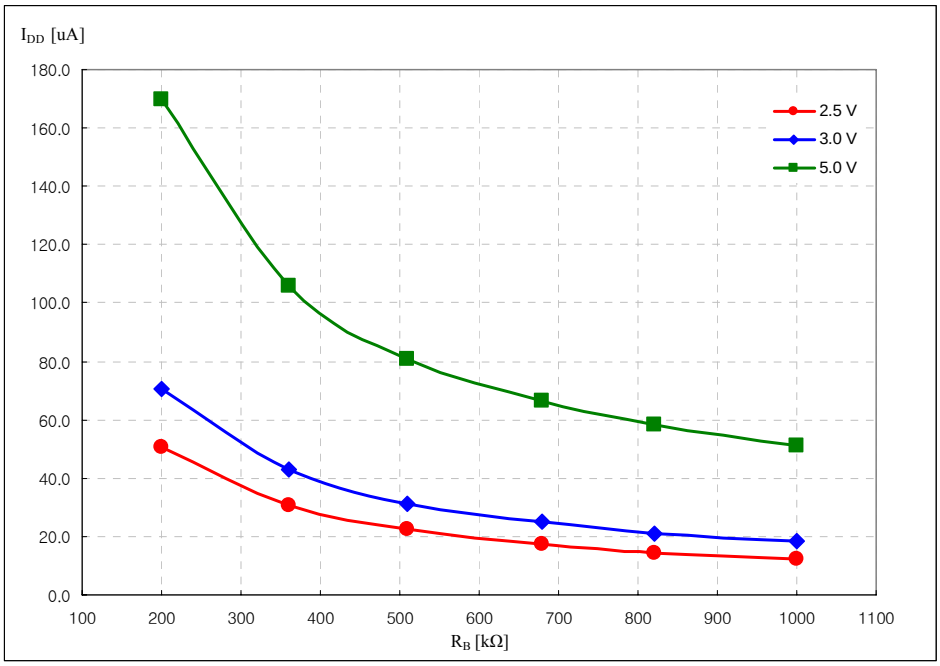
6 Implementation of TS06

6.1 RBIAS & SRBIAS implementation



The RBIAS is connected to the resistor to decide the oscillator and internal bias current. The sensing frequency, internal clock frequency and current consumption are therefore can be adjusted with R_B. A voltage ripple on RBIAS can make critical internal error, so C_B is connected to the VDD (not GND) is recommended. (The typical value of C_B is 820pF and the maximum Value is 1nF.)

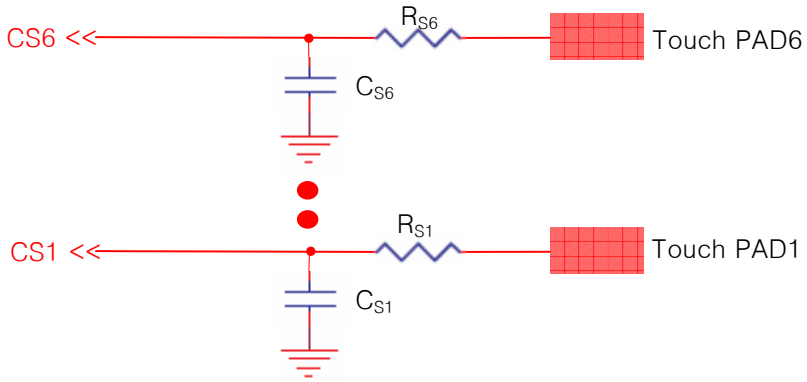
The R_{SB} should be connected as above figure when the TS06 operates in IDLE Mode to save the current consumption. In this case, not only the current consumption but also internal clock speed depends on the sum of the serial resistors, so that the response time might be longer.



Normal operation current consumption curve (@ Pin1 I2C_EN is High)

The current consumption curve of TS06 is represented in accordance with R_B value as above. The lower R_B requires more current consumption but it is recommended in noisy application. For example, refrigerator, air conditioner and so on.

6.2 CS implementation



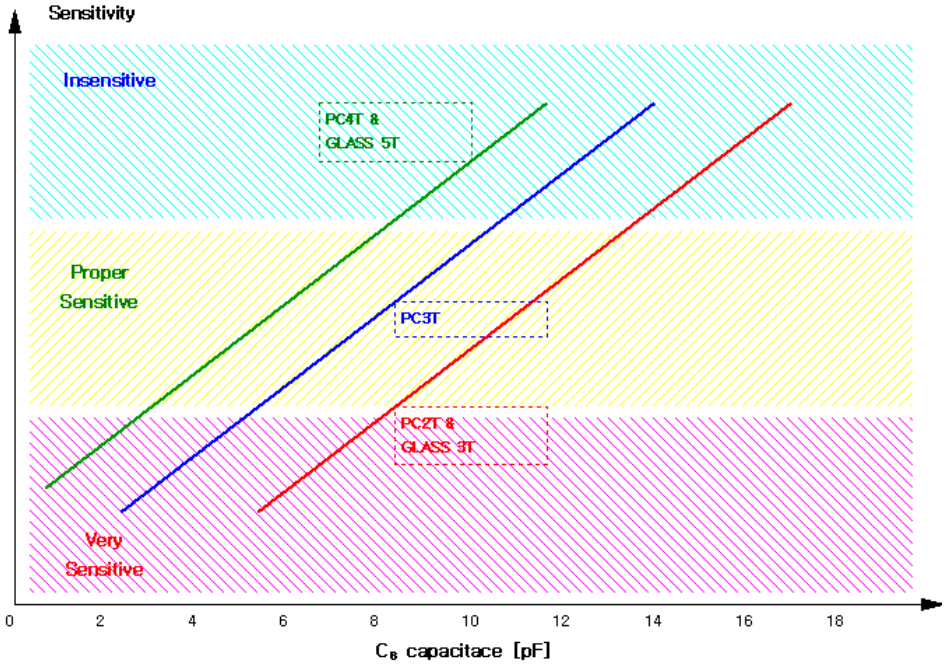
The TS06 has an available sensing channel up to 6, and each channel has 16 steps sensitivity which is available to control with internal register by I^2C interface. The parallel capacitor C_{S1} is added to CS1 and C_{S6} to CS6 to adjust fine sensitivity. The sensitivity would increased when a smaller value of C_S is used. (Refer to the below Sensitivity Example Figure) It could be useful in case detail sensitivity mediation is required. The internal touch decision process of each channel is separated from each other. The six channel touch key board application can therefore be designed by using only one TS06 without coupling problem. The R_S is serial connection resistor to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS1 ~ CS6 to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line.

There are some sensitivity difference among CS1, CS2 and CS3, and CS4, CS5 and CS6 caused by internal parasitic capacitance. That sensitivity difference could be compensated by using different C_S capacitor or sensitivity setting with internal register. To use different touch pattern area could be used for sensitivity compensation but not recommended. The sensitivity of each channel can be represented as below.

Sensitivity of CS1 ≥ Sensitivity of CS2, CS3 > Sensitivity of CS4, CS5, CS6
(In case of the external parasitic capacitance value is same on each channel.)

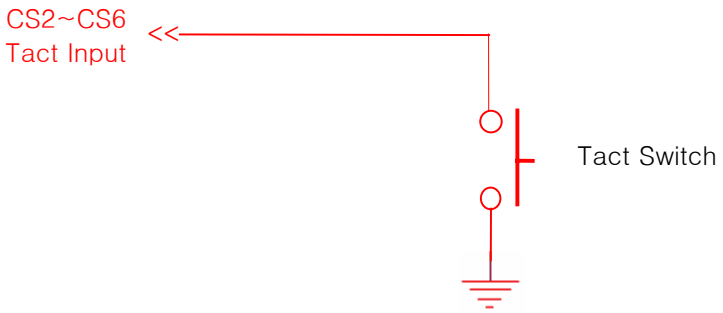
C_{CS1_PARA} + about 3.5pF = $C_{CS2,3\_PARA}$ + about 3pF = $C_{CS4,5,6\_PARA}$

* C_{CS1_PARA} : Parasitic capacitance of CS1
* $C_{CS2,3\_PARA}$: Parasitic capacitance of CS2 and CS3
* $C_{CS4,5,6\_PARA}$: Parasitic capacitance of CS4, CS5 and CS6



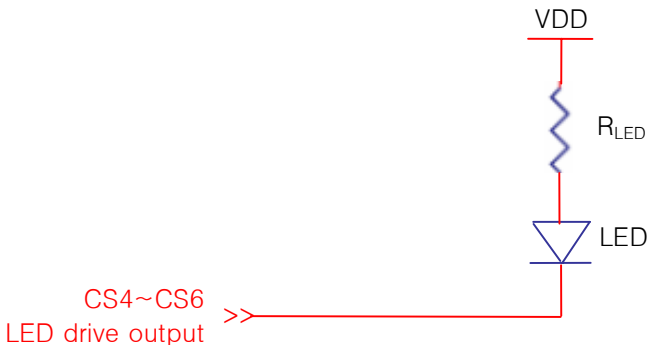
Sensitivity example figure with default sensitivity selection

6.3 CS implementation for tact input (CS2, CS3, CS4, CS5, CS6)



The TS06 has five CS input ports (from CS2 to CS6) for getting tact switch input. When key Input board designed by using touch sensor and tact switch inputs, the input mode might be changed by dedicated registers and the output also could get from output registers. When the CS used for tact switch input, the internal pull-up current source make it possible without external pull-up resistors. Typical internal pull-up current is 8uA independent to external condition

6.4 CS implementation for LED drive output (CS4, CS5, CS6)



The ports from CS4 to CS6 are available to use for LED drive output. When the application is required to be designed with LED display, the LED could be driven via CS4, CS5 or CS6. The LED drive output mode selection is available to control with internal register by I^2C interface. 32 steps LED dimming is also available with internal register by I^2C interface control. The maximum current that is sunk by CS is 20mA when the CS is used for LED drive output port.

6.5 Internal reset operation

The TS06 has stable internal reset circuit to offer reset pulse to digital block. The supply voltage for a system start or restart should be under $0.3 \cdot V_{DD}$ of normal operation V_{DD}. No external components required for TS06 power reset, that helps simple circuit design and to realize the low cost application.

6.6 Pattern Sleep ™

The purpose of pattern sleep is to remove unlock key in the application. For example, many mal-functions could happen if the mobile product is in the pocket. But thanks to the pattern sleep, the MCU would be awaken from IDLE mode with a proper touch input only.
The TS06 triggers the interrupt when it is touch on or touch off in normal operation. But the interrupt would be used when the touch inputs correspond with the reserved sequence in pattern sleep mode. And all the touch inputs should arrive within the expire time that is controllable by the dedicated register. As already mentioned, there is an advantage for the material cost as it will accordingly remove the unlock tact switch.
The pattern sleep function is allowed for the channel 1, 2, 3 and 4. (See Chapter 10)

** Pattern sleep setting up **
- Two types of pattern sleep mode could be provided.

Pattern Sleep Mode Type	Description
Slide Type	When the touch input sequence is coming by sliding touch. TP_SEL = 0
Touch to Touch Type	When the touch input sequence is coming by touch on / off TP_SEL = 1

- Expire time is available to control with PAT_EXPIRE_TIME register. (See Register Description)

- User defined pattern sequence

The interrupt generation is done by the OR operation between PAT_Ax and PAT_Bx in pattern sleep mode. The pattern is available to extend up to 8 steps.

Step1	PATTERN_A1	PATTERN_B1
Step2	PATTERN_A2	PATTERN_B2
Step3	PATTERN_A3	PATTERN_B3
Step4	PATTERN_A4	PATTERN_B4
Step5	PATTERN_A5	PATTERN_B5
Step6	PATTERN_A6	PATTERN_B6
Step7	PATTERN_A7	PATTERN_B7
Step8	PATTERN_A8	PATTERN_B8

* ATTENTION: The interrupt would be consecutively occurred if the values of PATTERN_A(1:8) or PATTERN_B(1:8) are same.

- Application support idea

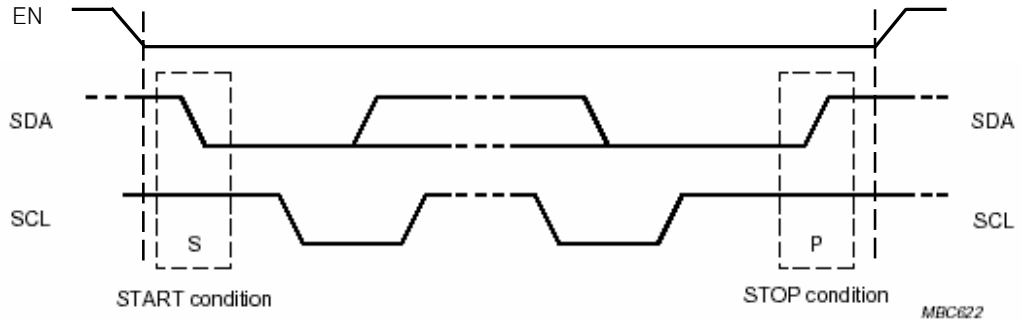
With our unique sleep pattern set up, it allows mobile phones, MP3 players and other devices to be in IDLE mode and then back to active mode using just a few easy steps. A mobile phone, for example, normally will be in left unattended in our pockets, tables, etc. Using our set up, mobile phones will automatically be in Idle mode without pressing any special keys. Sleep time (length of time before it goes to sleep) will vary depending on the time you input in the system. This will help prevent unnecessary dialed numbers or unwanted calls. Our sleep pattern set up will eliminate the use of special keys (e.g unlock key button) and instead it uses a touch sensors to activate and unlock the phone.

7 I²C Interface

7.1 Start & Stop Condition

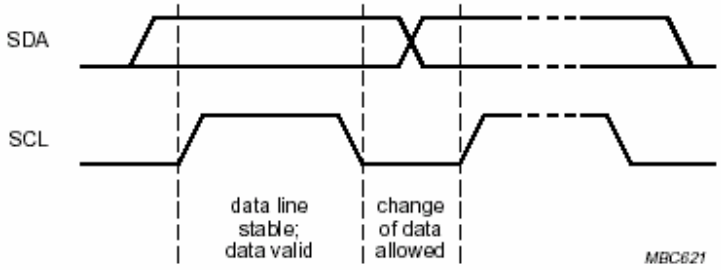
- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)

The EN (Pin1) should be low before START condition and be high after STOP condition.
The START condition should be appear after 2usec (minimum) from EN becomes Low.



7.2 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

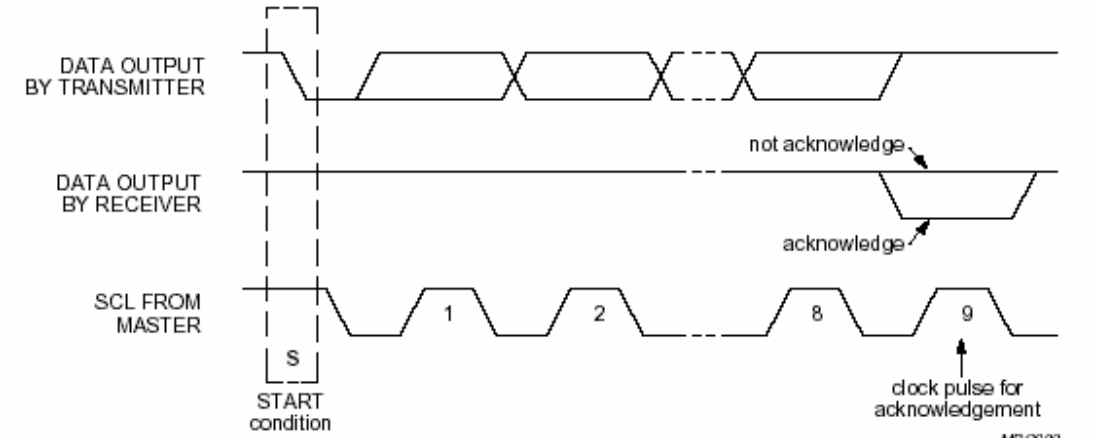


7.3 Byte Format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.4 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write '0' when it received the data successfully and '1' if not.



7.5 First Byte

7.5.1 Slave Address

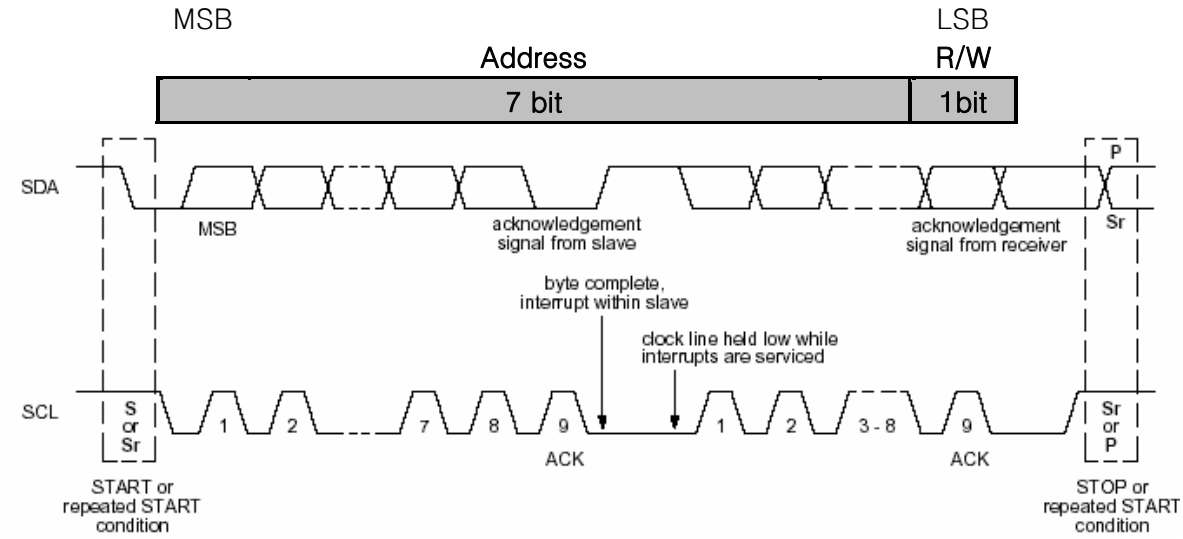
It is the first byte from the start condition. It is used to access the slave device.

TS06 Chip Address : 7bit

ID_SEL(CS1 Pin6)	Address
SENSING	0xD2
GND	0xF2

7.5.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.

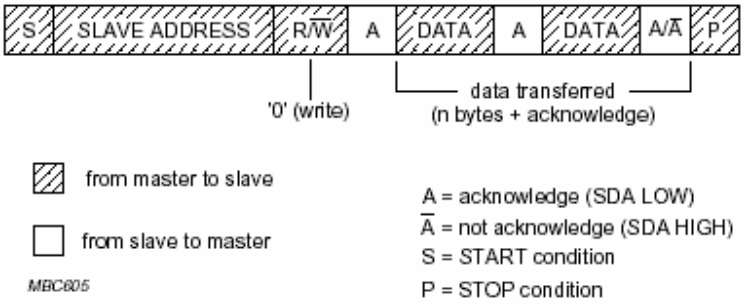


7.6 Transferring Data

7.6.1 Write Operation

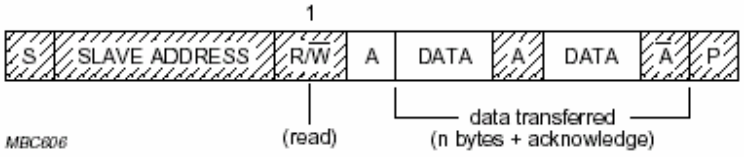
The byte sequence is as follows:

■ the first byte gives the device address plus the direction bit (R/W = 0).
■ the second byte contains the internal address of the first register to be accessed.
■ the next byte is written in the internal register. Following bytes are written in successive internal registers.
■ the transfer lasts until stop conditions are encountered.
■ the TS06 acknowledges every byte transfer.

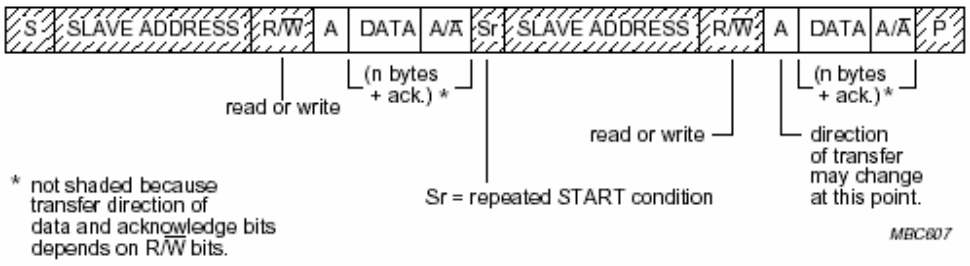


7.6.2 Read Operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.6.3 Read/Write Operation



7.7 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0xD2	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

Read register 0x00 and 0x01

Start	Device Address 0xD2	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0xD3	ACK	Data Read AA	ACK	Data Read BB	$\overline{\text{ACK}}$	Stop

From Master to Slave

From Slave to Master

8 TS06 Register List

◂ Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.
◂ Note: The bit0 and bit1 of CTRL2 register must be written by 0b11 after power on during an initialize phase. (Refer to the chapter 9. initialize flow)
◂ Note: HS (High Sensitivity) / MS (Middle Sensitivity) / LS (Low Sensitivity)
◂ Note: Low Output (light touch) / Middle Output (middle touch) / High Output (hard touch)

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sensitivity1	00h	0101 0101	SEN_CH2				SEN_CH1			
Sensitivity2	01h	0101 0101	SEN_CH4				SEN_CH3			
Sensitivity3	02h	0101 0101	SEN_CH6				SEN_CH5			
CTRL1	03h	0000 1010	–	–	MS	FTC		RTC		
CTRL2	04h	0001 0010	–	LED_EN	S/M_SEL	IMP_SEL	SRST	SLEEP	1	1
Ref_Rst	05h	0011 1000	–	–	CH6	CH5	CH4	CH3	CH2	CH1
Ch_Hold	06h	0011 100X	–	–	CH6	CH5	CH4	CH3	CH2	1
Cal_Hold	07h	0000 0000	–	–	CH6	CH5	CH4	CH3	CH2	CH1
Dome_En	08h	0000 0000	–	–	–	CH6	CH5	CH4	CH3	CH2
Cal_Ctrl	09h	1111 1101	BF_UP		BF_DOWN		BS		SLEEP	
Pat_Ctrl	0Ah	0000 0000	SM_SEL	TP_SEL	ETS	PAT_EXPIRE_TIME				
Pat_A0	0Bh	0000 0000	PATTERN_A2				PATTERN_A1			
Pat_A1	0Ch	0000 0000	PATTERN_A4				PATTERN_A3			
Pat_A2	0Dh	0000 0000	PATTERN_A6				PATTERN_A5			
Pat_A3	0Eh	0000 0000	PATTERN_A8				PATTERN_A7			
Pat_B0	0Fh	0000 0000	PATTERN_B2				PATTERN_B1			
Pat_B1	10h	0000 0000	PATTERN_B4				PATTERN_B3			
Pat_B2	11h	0000 0000	PATTERN_B6				PATTERN_B5			
Pat_B3	12h	0000 0000	PATTERN_B8				PATTERN_B7			
PWM0	13h	0000 0000	PWM_OUT_CH4							
PWM1	14h	0000 0000	PWM_OUT_CH5							
PWM2	15h	0000 0000	PWM_OUT_CH6							
Output0	25h	00000000	–	ND	CH6	CH5	CH4	CH3	CH2	CH1

8.2 Sensitivity Control Register

Sensitivity1 Channel 1 & 2 Sensitivity Control

Address (hex): 00h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEN_CH2[3:0]				SEN_CH1[3:0]			

Description

The sensitivity of channel 1 and 2 are adjustable by Sensitivity1 register.

Bit name	Reset	Function
SEN_CHx[3:0]	0101	Sensitivity T (= thickness of PC) of Channel 1 @Cs = 0pF 0000: 11.0 ~ 15.0T 0001: 9.0 ~ 12.0T 0010: 8.0 ~ 10.0T 0011: 7.0 ~ 8.5T 0100: 6.0 ~ 7.5T 0101: 5.5 ~ 7.0T 0110: 5.0 ~ 6.5T 0111: 4.5 ~ 6.0T 1000: 4.25 ~ 5.50T 1001: 4.00 ~ 5.25T 1010: 3.75 ~ 5.00T 1011: 3.50 ~ 4.75T 1100: 3.25 ~ 4.50T 1101: 3.00 ~ 4.25T 1110: 2.75 ~ 4.00T 1111: 2.50 ~ 3.75T Sensitivity T (= thickness of PC) of Channel 2 @Cs = 0pF 0000: 8.0 ~ 11.0T 0001: 7.0 ~ 9.0T 0010: 6.0 ~ 7.5T 0011: 5.0 ~ 6.5T 0100: 4.5 ~ 6.0T 0101: 4.0 ~ 5.5T 0110: 3.75 ~ 5.00T 0111: 3.50 ~ 4.75T 1000: 3.25 ~ 4.50T 1001: 3.00 ~ 4.25T 1010: 2.75 ~ 4.00T 1011: 2.50 ~ 3.75T 1100: 2.25 ~ 3.50T 1101: 2.00 ~ 3.25T 1110: 1.80 ~ 3.00T 1111: 1.60 ~ 2.75T

Sensitivity2 Channel 3 & 4 Sensitivity Control

Address (hex): 01h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEN_CH4[3:0]				SEN_CH3[3:0]			

Description

The sensitivity of channel 3 and 4 are adjustable by Sensitivity2 register.

Bit name	Reset	Function
SEN_CHx[3:0]	0101	Sensitivity T (= thickness of PC) of Channel 3 @Cs = 0pF 0000: 8.0 ~ 11.0T 0001: 7.0 ~ 9.0T 0010: 6.0 ~ 7.5T 0011: 5.0 ~ 6.5T 0100: 4.5 ~ 6.0T 0101: 4.0 ~ 5.5T 0110: 3.75 ~ 5.00T 0111: 3.50 ~ 4.75T 1000: 3.25 ~ 4.50T 1001: 3.00 ~ 4.25T 1010: 2.75 ~ 4.00T 1011: 2.50 ~ 3.75T 1100: 2.25 ~ 3.50T 1101: 2.00 ~ 3.25T 1110: 1.80 ~ 3.00T 1111: 1.60 ~ 2.75T
		Sensitivity T (= thickness of PC) of Channel 4 @Cs = 0pF 0000: 6.0 ~ 8.0T 0001: 5.0 ~ 6.5T 0010: 4.5 ~ 6.0T 0011: 4.0 ~ 5.5T 0100: 3.5 ~ 5.0T 0101: 3.0 ~ 4.5T 0110: 2.75 ~ 4.00T 0111: 2.50 ~ 3.75T 1000: 2.25 ~ 3.50T 1001: 2.00 ~ 3.25T 1010: 1.80 ~ 3.00T 1011: 1.60 ~ 2.75T 1100: 1.40 ~ 2.50T 1101: 1.20 ~ 2.25T 1110: 1.00 ~ 2.00T 1111: 1.00 ~ 1.80T

Sensitivity3 Channel 5 & 6 Sensitivity Control

Address (hex): 02h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEN_CH6[3:0]				SEN_CH5[3:0]			

Description

The sensitivity of channel 5 and 6 are adjustable by Sensitivity3 register.

Bit name	Reset	Function
SEN_CHx[3:0]	0101	Sensitivity T (= thickness of PC) of Channel 5, 6 @Cs = 0pF 0000: 6.0 ~ 8.0T 0001: 5.0 ~ 6.5T 0010: 4.5 ~ 6.0T 0011: 4.0 ~ 5.5T 0100: 3.5 ~ 5.0T 0101: 3.0 ~ 4.5T 0110: 2.75 ~ 4.00T 0111: 2.50 ~ 3.75T 1000: 2.25 ~ 3.50T 1001: 2.00 ~ 3.25T 1010: 1.80 ~ 3.00T 1011: 1.60 ~ 2.75T 1100: 1.40 ~ 2.50T 1101: 1.20 ~ 2.25T 1110: 1.00 ~ 2.00T 1111: 1.00 ~ 1.80T

8.3 General Control Register1

CTRL1 TS06 General Control Register1

Address (hex): 03h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	MS	FTC[1:0]		RTC[2:0]		

Description

The calibration speed just after power on reset is very high during the time which is defined by FTC[1:0] to have a good adoption against unstable external environment.

Bit name	Reset	Function
MS	0	Mode Selection 0: auto alternate (fast/slow) mode 1: fast mode
FTC[1:0]	01	First Touch Control Below time stands on VDD = 3V / Rb = 420KΩ 00: 5 sec 01: 10 sec 10: 15 sec 11: 20 sec
RTC[2:0]	010	Response Time Control Response period = RTC[2:0] + 2

8.4 General Control Register2

CTRL2 TS06 General Control Register2

Address (hex): 04h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	LED_EN	S/M_SEL	IMP_SEL	SRST	SLEEP	1	1

Description

All the digital blocks except analog and I^2C block are reset when SRST is set. The SLEEP function allows getting very low current consumption when it is set. But the response time will be longer than normal operation.

Bit name	Reset	Function
LED_EN	0	LED Enable / Disable Control 0: LED Drive Disable 1: LED Drive Enable
S/M_SEL	0	Single/Multi Mode Select 0: Multi Mode 1: Single Mode
IMP_SEL	1	Impedance Select 0: Low Impedance 1: High Impedance
SRST	0	Software Reset 0: Disable Software Reset 1: Enable Software Reset
SLEEP	0	Sleep Mode Enable 0: Disable Sleep Mode 1: Enable Sleep Mode

8.5 Channel Reference Reset Control Register

Ref_rst Channel1~6 Reference Reset Control

Address (hex): 05h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

Description

The reference value of each channel will be renewing when Chx is set.

Bit name	Reset	Function
Ch(1:3)	000	0: Disable reference reset 1: Enable reference reset
Ch(4:6)	111	0: Disable reference reset 1: Enable reference reset

8.6 Channel 1~6 Sensing Control Register

Ch_hold Channel 1 ~ 6 Hold Enable Register

Address (hex): 06h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	Ch6	Ch5	Ch4	Ch3	Ch2	X

Description

The operation of each channel is independently available to control. A channel doesn't be worked and the calibration is paused when it is set.

The hold function is not available for channel 1(Bit0).

Bit name	Reset	Function
Ch(2:3)	000	0: Enable operation (sensing + calibration) 1: Hold operation (No sensing + Stop calibration)
Ch(4:6)	111	0: Enable operation (sensing + calibration) 1: Hold operation (No sensing + Stop calibration)

8.7 Channel 1~6 Calibration Control Register

Cal_hold Channel 1 ~ 6 Calibration Enable Register

Address (hex): 07h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

Description

The calibration of each channel is independently available to control. Each channel is working even if a bit is set.

Bit name	Reset	Function
Chx	0	0: Enable reference calibration (sensing + calibration) 1: Disable reference calibration (sensing + No calibration)

8.8 Channel 2~6 Dome Key Input Control Register

Dome_en Channel 2 ~ 6 Dome Key Enable Register

Address (hex): 08h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	Ch6	Ch5	Ch4	Ch3	Ch2

Description

The tact key input is available to control with Dome_en register.

Bit name	Reset	Function
Chx	0	0: Disable tact key input

		1: Enable tact key input

8.9 Calibration Speed Control Register

Cal_ctrl Calibration Speed Control Register

Address (hex): 09h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BF_UP		BF_DOWN		BS		SLEEP	

Description

The calibration speed might be controlled on each operation mode by Cal_ctrl register.

Bit name	Reset	Function
BF_UP[1:0]	11	Calibration speed control upper direction in BF mode 00: Fastest 01: Fast 10: Normal 11: Slow
BF_DOWN[1:0]	11	Calibration speed control lower direction in BF mode 00: Fastest 01: Fast 10: Normal 11: Slow
BS[1:0]	11	Calibration speed control in BS mode (up, Down) 00: Fastest 01: Fast 10: Normal 11: Slow
SLEEP[1:0]	01	Calibration speed control in SLEEP mode (up, Down) 00: Fast 01: Normal 10: Slow 11: Not Use

8.10 Pattern function Control Register

Pat_ctrl Pattern Function Control Register

Address (hex): 0Ah

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SM_SEL	TP_SEL	ETS	PAT_EXPIRE_TIME				

Description

The pattern sleep function is might be controlled by Pat_ctrl register. In case of the sliding type pattern interrupt, TP_SEL = 0 selection could have more advantage and TP_SEL = 1 selection is useful when the pattern be required to check touch on and off detection.

Bit name	Reset	Function
SM_SEL	0	Sleep mode select

		0: Normal Sleep Mode 1: Pattern Sleep Mode
TP_SEL	0	Touch pattern select 0: Compare the pattern with only touch on detection 1: Compare the pattern with touch on and off detection
ETS	0	Expire Time Speed control 0: Expire Time Speed = 1 1: Expire Time Speed = 8
PAT_EXPIRE_TIME [4:0]	00000	The intelligent pattern algorithm will wait for the end of pattern input for the time that is set by pattern expire time register. Expire Time = Infinite when PAT_EXPIRE_TIME [4:0] is 00000 Expire Time = PAT_EXPIRE_TIME[4:0] x 80ms x Expire Time Speed

8.11 **Pattern A Selection Register**

Pat_A(0~3) Pattern A Selection Registers

Address (hex): 0Bh
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_A2				PATTERN_A1			

Address (hex): 0Ch
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_A4				PATTERN_A3			

Address (hex): 0Dh
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_A6				PATTERN_A5			

Address (hex): 0Eh
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_A8				PATTERN_A7			

Description
The depth of pattern A could be extended up to 8 steps.

Bit name	Reset	Function
PATTERN_An[3:0]	0000	PATTERN_An[3] are pattern data that is compared with CH4 output. PATTERN_An[2] are pattern data that is compared with CH3 output. PATTERN_An[1] are pattern data that is compared with CH2 output. PATTERN_An[0] are pattern data that is compared with CH1 output. ※ The n of An indicates the number of pattern steps.

8.12 Pattern B Selection Register

Pat_B(0~3) Pattern B Selection Registers

Address (hex): 0Fh
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_B2				PATTERN_B1			

Address (hex): 10h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_B4				PATTERN_B3			

Address (hex): 11h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_B6				PATTERN_B5			

Address (hex): 12h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PATTERN_B8				PATTERN_B7			

Description
The depth of pattern B could be extended up to 8 steps.

Bit name	Reset	Function
PATTERN_Bn[3:0]	0000	PATTERN_Bn[3] are pattern data that is compared with CH4 output. PATTERN_Bn[2] are pattern data that is compared with CH3 output. PATTERN_Bn[1] are pattern data that is compared with CH2 output. PATTERN_Bn[0] are pattern data that is compared with CH1 output. ※ The n of Bn indicates the number of pattern steps.

8.13 PWM Control Register

PWM(0~2) LED Dimming Control Registers

Address (hex): 13h ~ 15h
Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	PWM_OUT_CH4 ~ CH6				

Description
The LED could be driven by TS06 within 32 steps.

Bit name	Reset	Function
PWM_OUT_CHx[4:0]	00000	LED dimming controllable up to 32 steps. 00000: The minimum luminance 11111: The maximum luminance

8.14 Output Register

Output Channel 1 ~ 6 Output Register

Address (hex): 25h

Type: R

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	ND	CH6	CH5	CH4	CH3	CH2	CH1

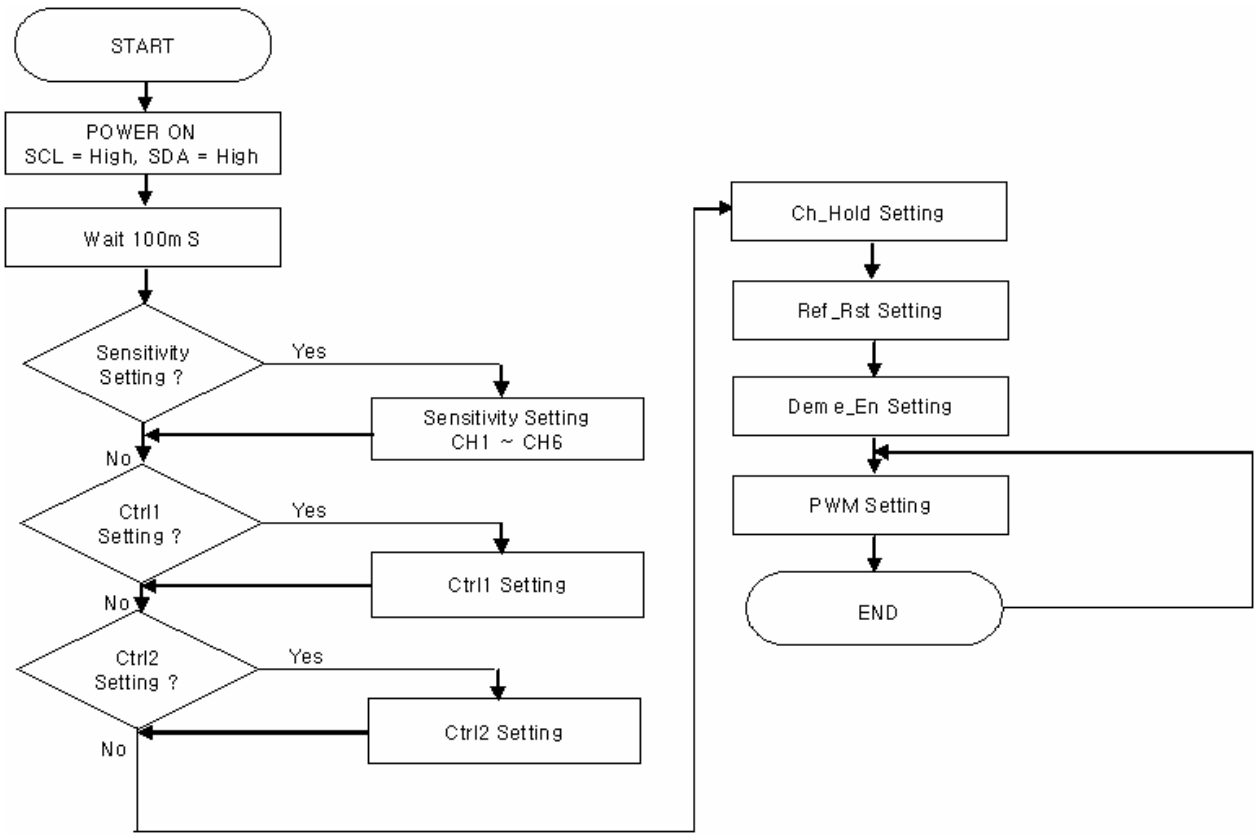
Description

The each channel output of TS06 is provided with 1 bit. It represents to detect result as below table.

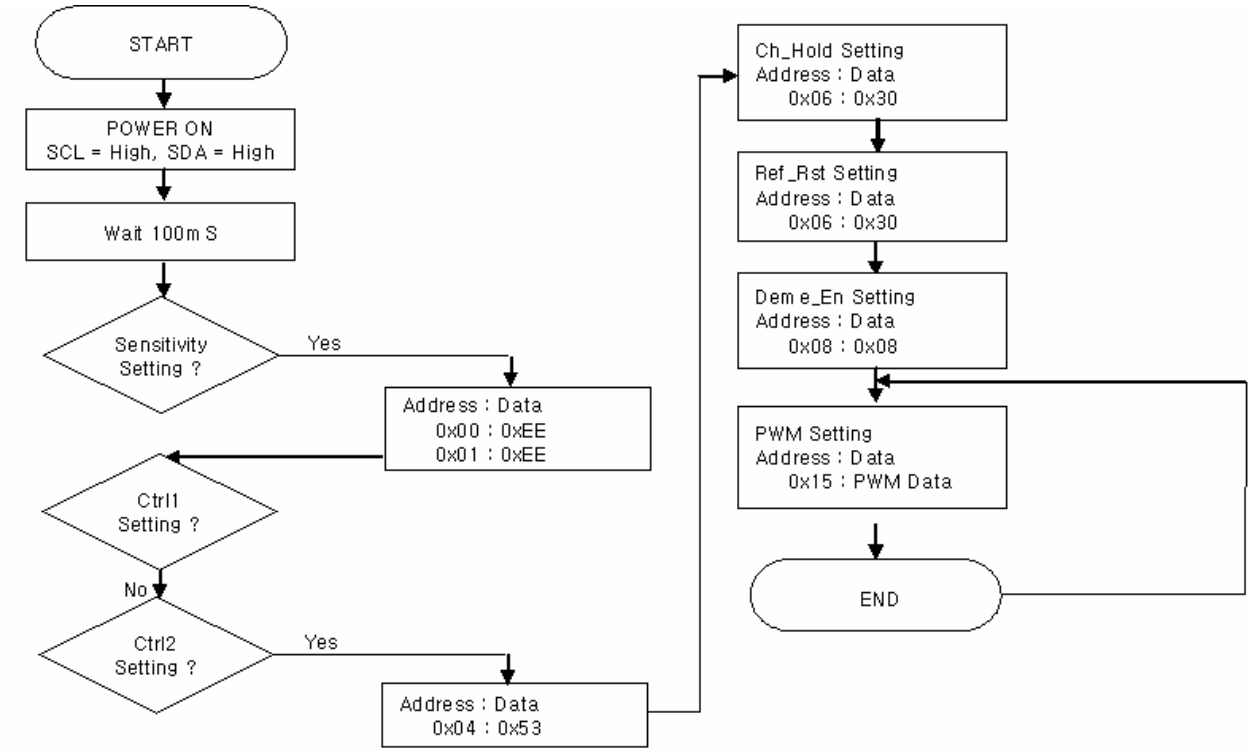
Bit name	Reset	Function
ND	0	Noise Detect Indication 0: Normal State 1: Noisy State
CHx	0	Output of channel x 0: No touch 1: Detected touch

9 Recommended TS06 Power Up Sequence (Example)

9.1 Recommended TS06 Power Up Flow Chart



9.2 Recommended TS06 Power Up Sequence Sample

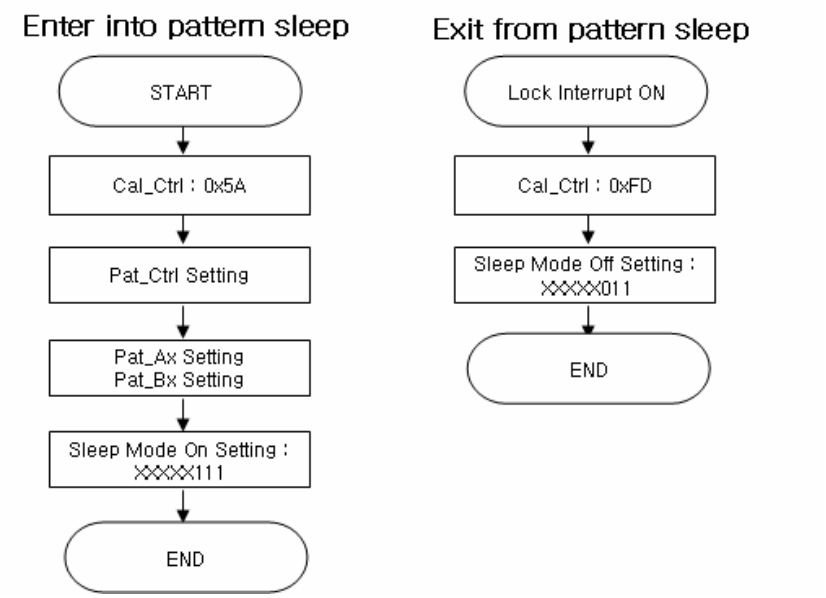


Sample Flow Chart

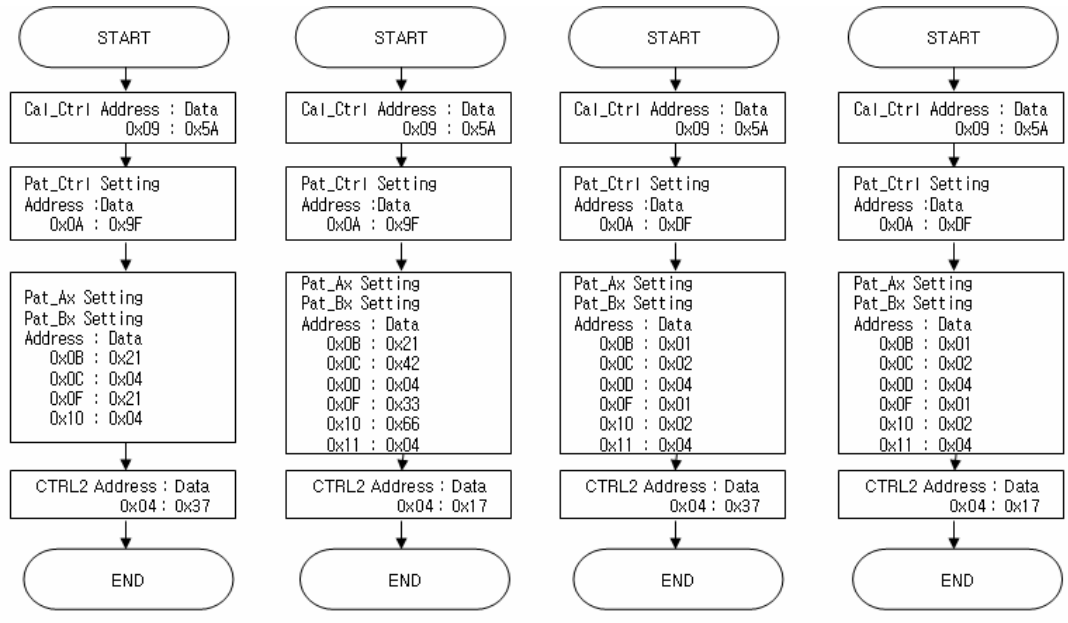
- CH1 ~ CH4 : Touch Sensor
- Sensitivity : All 2.0%
- CH5 : Tact Switch
- CH6 : LED Driver

10 Recommended TS06 Pattern Sleep Sequence (Example)

10.1 Recommended TS06 Pattern Sleep Flow Chart



10.2 Recommended TS06 Pattern Sleep Sequence to enter



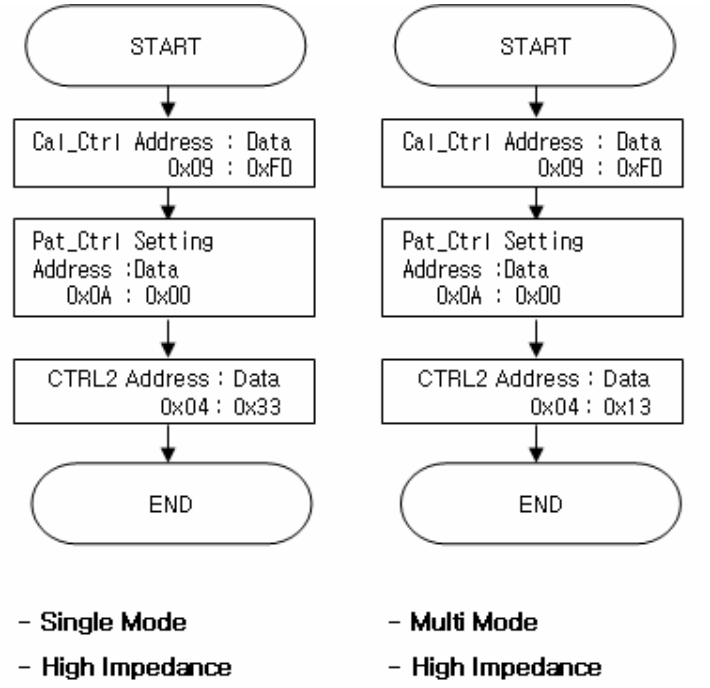
- Single Mode
- Uncheck Touch Off
- Expired Time : 2.5S

- Multi Mode
- Uncheck Touch Off
- Expired Time : 2.5S

- Single Mode
- Check Touch Off
- Expired Time : 2.5S

- Multi Mode
- Check Touch Off
- Expired Time : 2.5S

10.3 Recommended TS06 Pattern Sleep Sequence to exit

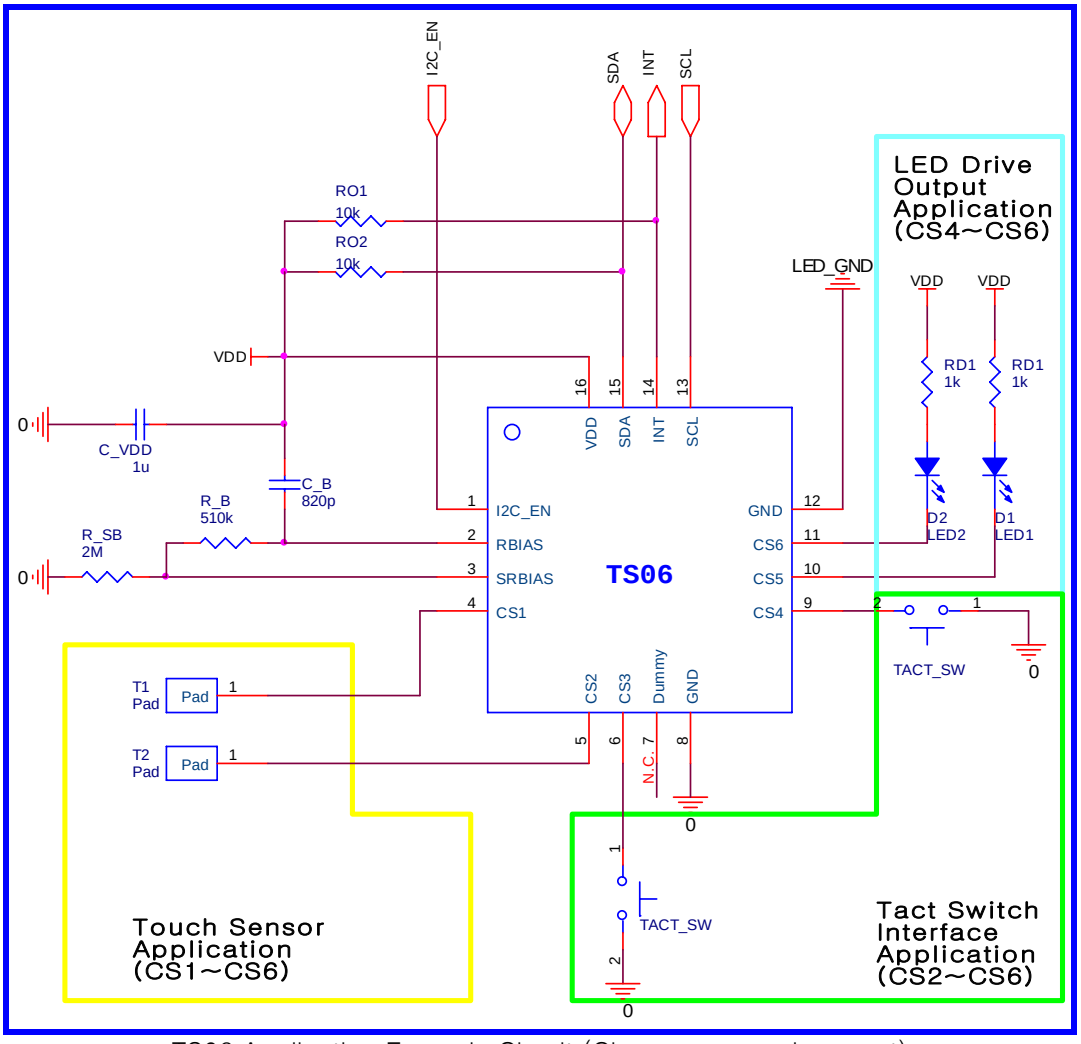


- Single Mode
- High Impedance

- Multi Mode
- High Impedance

11 Recommended Circuit Diagram

11.1 Application Example in clean power environment

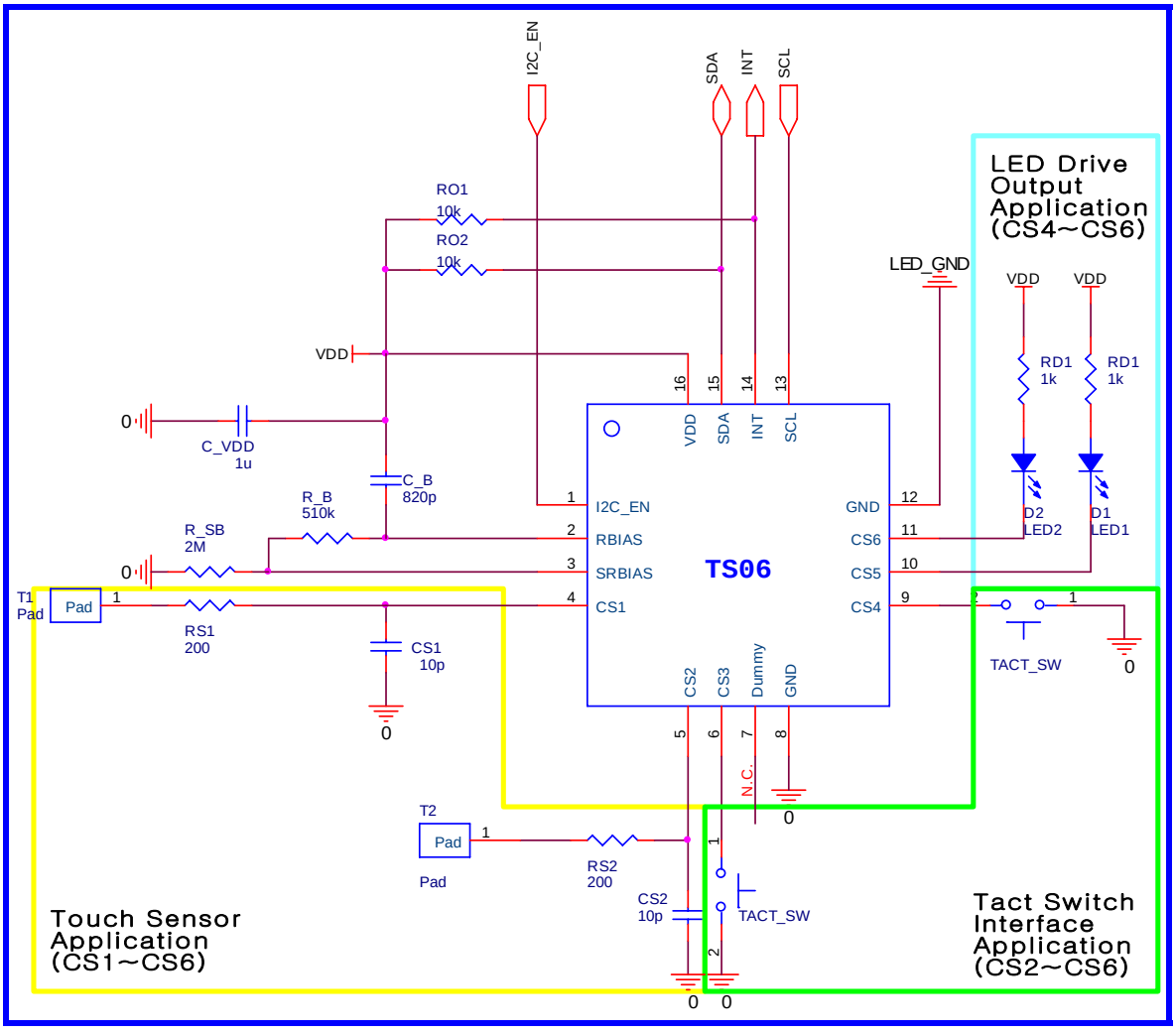


TS06 Application Example Circuit (Clean power environment)

- In PCB layout, R_B should not be placed on touch pattern. If not, C_B has to be connected. The R_B pattern should be routed as short as possible.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm (or narrower line).
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS06.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The TS06 is reset when power rise from 0V to proper VDD

- The LED_GND and GND should be short in the system and the lines are recommended to be split from the most low impedance ground point to avoid ground bouncing problems.

11.2 Application Example in noisy environment

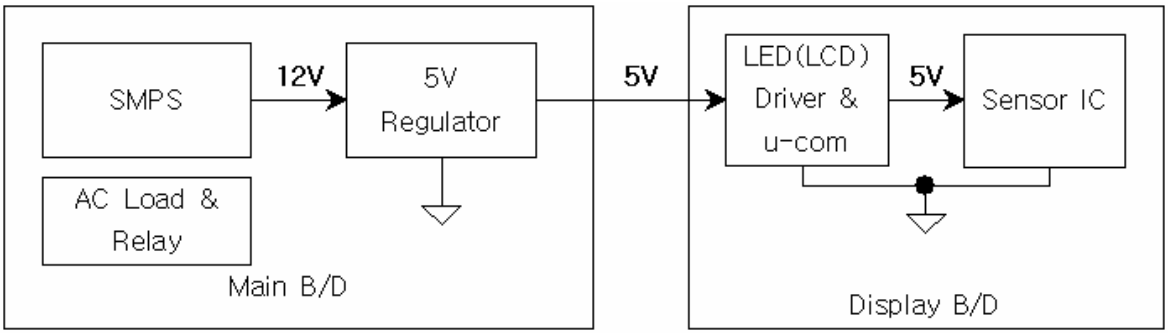


TS06 Application Example Circuit (Noisy environment)

- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The smaller R_B is recommended in noisy environments.
- Thanks to the RS1, RS2, CS1 and CS2, the noise immunity could be improved.
- The LED_GND and GND should be short in the system and the lines are recommended to be split from the most low impedance ground point to avoid ground bouncing problems.

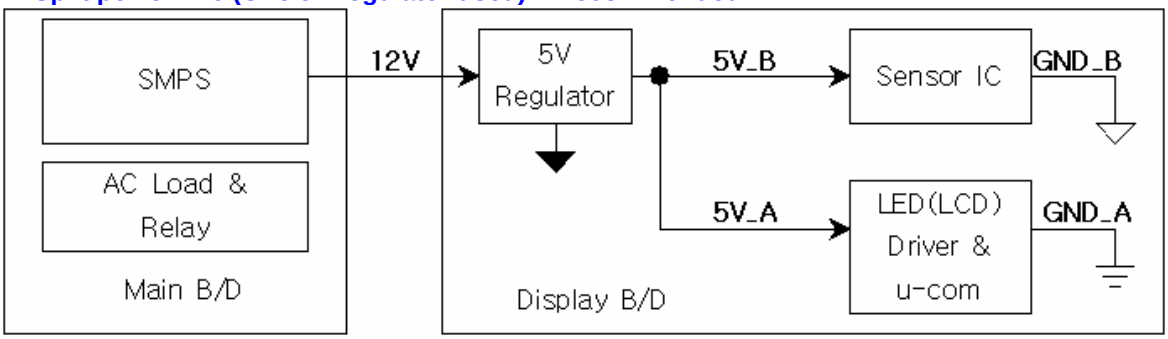
11.3 Example – Power Line Split Strategy PCB Layout

A. Not split power line (Bad power line design)

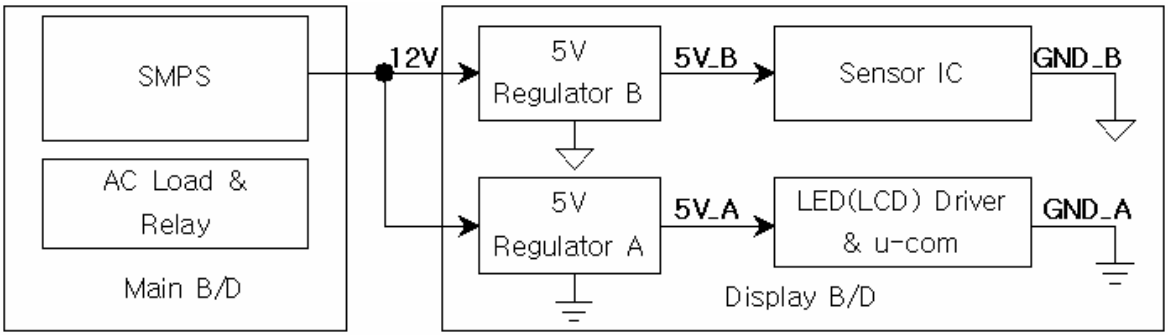


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

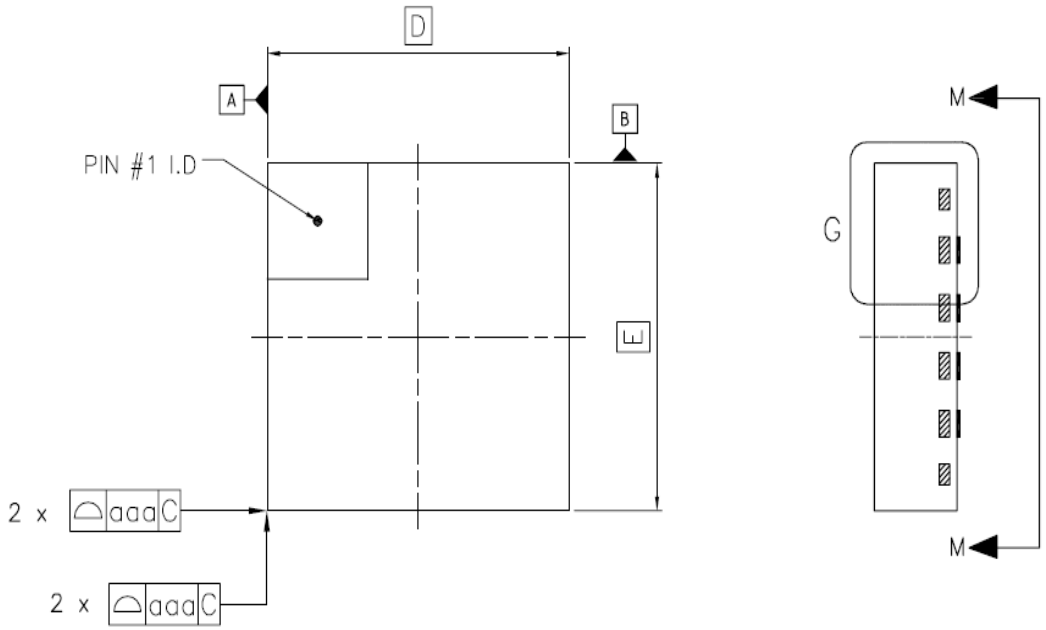
B. Split power line (One 5V regulator used) – Recommended

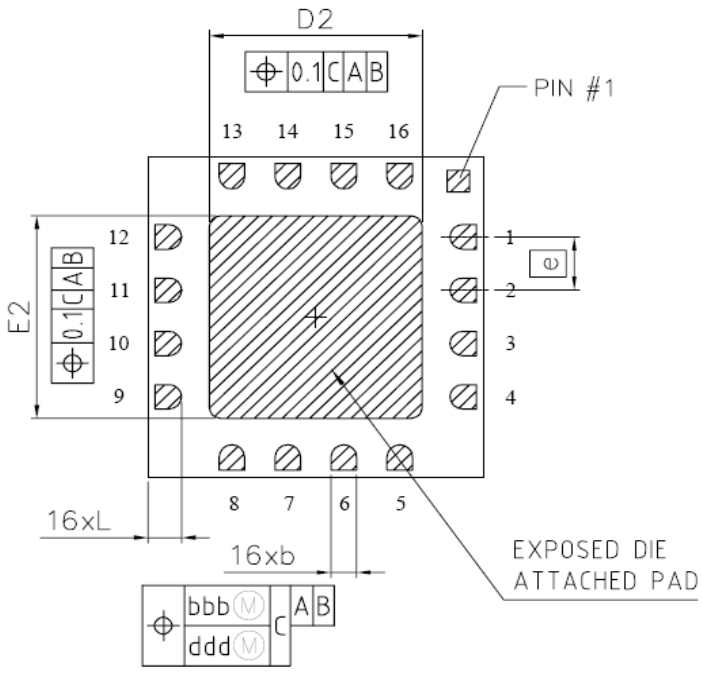


C. Split power line (Separated 5V regulator used) – Strongly recommended

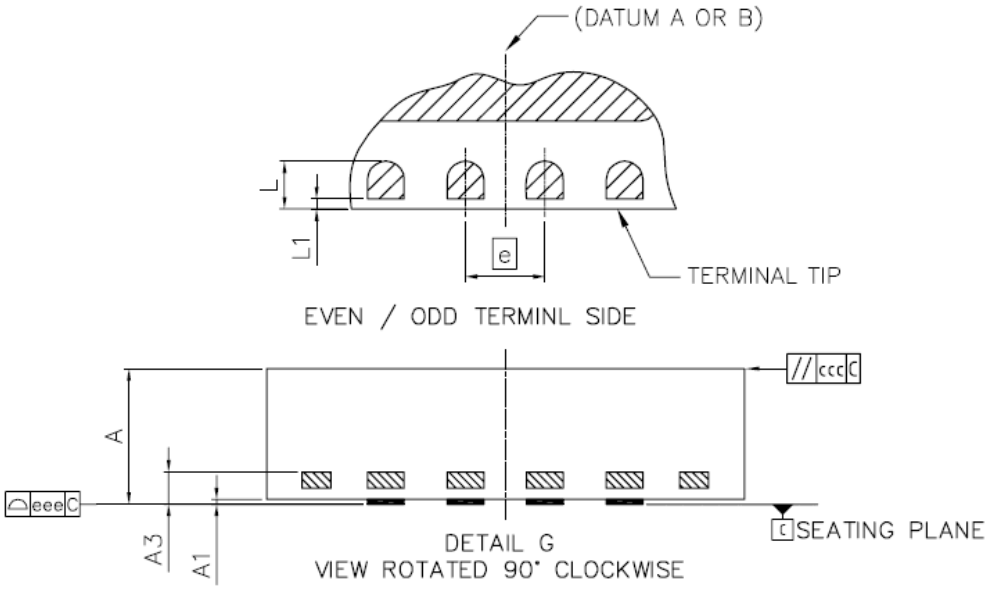


12 MECHANICAL DRAWING





VIEW M–M



DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.18	0.23	0.28
D		3.00 BSC	
E		3.00 BSC	
D2	1.80	1.90	2.00
E2	1.80	1.90	2.00
e		0.50 BSC	
L	0.25	0.30	0.35
L1	0.00		0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

13 MARKING DESCRIPTION

Device Code : **T S 0 6**

Channel Number
Touch Switch Group

Weekly Code : **YY WW**

Manufacturing Year
Manufacturing Week

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